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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,923	01/12/2005	Kazuya Kamitake	50395-305	4825

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/520,923	KAMITAKE ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-17 and 21-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-17 and 21-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/520923 Attorney's Docket #: 50395-305
Filing Date: 1/12/2005; claimed foreign priority to 7/17/2002 & 4/2/2003

Applicant: Kamitake et al.

Examiner: Alexander Williams

This application is a 371 of PCT/JP03/08624 filed 7/7/2003.

Applicant's Amendment filed 10/29/2007 has been acknowledged.

Claims 1-11 and 18-20 have been cancelled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 12-17 and 21-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent # 5,276,351) in view of Hirose et al. (Japan Patent Publication # 10-284643).

12. Yamazaki et al. (figures 1 to 9) specifically figure 2 show a member for a semiconductor device comprising a base member **21a** made of an alloy or composite mainly composed of Cu and W and/or Mo, wherein a coating layer **30** made of a hard carbon film is provided on at least a surface of the base member on which another member for the semiconductor device is bonded with a resin **31**, but fail to explicitly show the coating layer has a thickness of 0.1 to 10 .mu.m. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

14. Yamazaki et al. (figures 1 to 9) specifically figure 2 show a member for a semiconductor device comprising a base member **21a** made of an alloy or composite mainly composed of Al--SiC, wherein a coating layer **30** made of a hard carbon film is provided on at least a surface of the base member on which another member for the semiconductor device is bonded with a resin **31**, but fail to explicitly show the coating layer has a thickness of 0.1 to 10 .mu.m. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

16. Yamazaki et al. (figures 1 to 9) specifically figure 2 show a member for a semiconductor device comprising a base member **21a** made of an alloy or composite mainly composed of Si--SiC, wherein a coating layer **30** made of a hard carbon film is provided on at least a surface of the base member on which another member for the semiconductor device is bonded with a resin **31**, but fail to explicitly show the coating layer has a thickness of 0.1 to 10 .mu.m. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

(35) A single layer consisting mainly of a material selected from the group consisting of silicon oxide, silicon carbide, silicon nitride, hard carbon and a mixture comprising such materials at a stoichiometric ratio or a non-stoichiometric ratio is suitable for the inorganic protective film and also a multi-layered film comprising such layers is suitable for the inorganic protective film. **The thickness thereof is preferably 30 to 500 nm.**

(2) FIG. 2 is a vertical sectional view showing a Flat Pack Package Type of a semiconductor device using the lead frame produced in accordance with the present invention. In FIG. 2, **a lead frame 21 made from 42 ALLOY or copper** comprises a die 21a for die-attaching a semiconductor chip 23, and a lead section, that is an inner lead 21b and an outer lead 21c. The surface of the die 21a and the inner lead 21b are covered with **an inorganic material 30** with the exception of the part on which the semiconductor chip 23 is mounted, and of a connection part 25 on which gold is printed for wire-bonding. The semiconductor chip 23 is electrically connected to a portion 25 of the inner lead 21b (where gold plating has been applied) through an aluminum pad 27 and a gold wire 29 for wire-bonding, and they are sealed by a molding 1.

(3) Next, the process for manufacturing the lead frame of the present invention will be explained with reference to FIGS. 3A to 3D.

(4) FIG. 3A is a sectional view of the lead frame which comprises a die 35 for mounting a semiconductor chip thereon, a lead section 37, a portion 39 on the lead section 37 for electrically connection by wire bonding, and a frame 41 for the lead frame. The die 35 is provided in a position lower than the lead section 37, so that a contact section provided on the chip is made on the same level or flush with the connecting portion 39. The lead frame is selectively subjected to a screen printing method in a region where it is not desired to form an inorganic protective film, specifically, on the upper surface of the die 35 on which the semiconductor chip is mounted and on the connecting portion 39 of the lead section, so that a cover 43 of organic resin such as epoxy resin or polyamide is formed thereon, as shown in FIG. 3B, by the screen printing method.

(5) Subsequently, as shown in FIG. 3C, a protective film of an inorganic material, such as silicon nitride, silicon oxide, silicon carbide, or DLC, is formed over the entire lead frame by a plasma CVD or sputtering method (which will later be explained in detail). The inorganic material must show no qualitative changes when held for one hour in air at 500.degree. C., must be heat-resistant, and must be resistant to oxidation. For this reason silicon nitride or silicon carbide are particularly superior for this application.

Hirose et al. is cited for showing a substrate for a semiconductor device. Specifically, Hirose et al. (figures 1 to 8) specifically figure discloses the coating layer has a thickness of 0.1 to 10 .mu.m. for the purpose of providing a sufficient resin bonding strength to be maintained.

13. The member for a semiconductor device according to claim 12, Yamazaki et al. show wherein the alloy or composite mainly composed of Cu and W and/or Mo contains Cu of 5 to 40% by weight.

15. The member for a semiconductor device according to claim 14, Yamazaki et al. show wherein the alloy or composite mainly composed of Al--SiC contains SiC of 10 to 70% by weight.

17. The member for a semiconductor device according to claim 16, Yamazaki et al. show wherein the alloy or composite mainly composed of Si--SiC contains Si of 10 to 35% by weight.

21. The member for a semiconductor device according to claim 12, Yamazaki et al. show wherein the surface of the base member on which the coating layer is formed has a surface roughness of 0.1 to 20 .mu.m in Rmax.

22. The member for a semiconductor device according to claim 14, Yamazaki et al. show wherein the surface of the base member on which the coating layer is formed has a surface roughness of 0.1 to 20 .mu.m in Rmax.

23. The member for a semiconductor device according to claim 16, Yamazaki et al. show wherein the surface of the base member on which the coating layer is formed has a surface roughness of 0.1 to 20 .mu.m in Rmax.

24. The member for a semiconductor device according to claim 12, Yamazaki et al. show wherein pores in the surface of the base member on which the coating layer is formed have a depth of 100 .mu.m or less.

25. The member for a semiconductor device according to claim 14, Yamazaki et al. show wherein pores in the surface of the

base member on which the coating layer is formed have a depth of 100 .mu.m or less.

26. The member for a semiconductor device according to claim 16, Yamazaki et al. show wherein pores in the surface of the base member on which the coating layer is formed have a depth of 100 .mu.m or less.

27. The member for a semiconductor device according to claim 12, Yamazaki et al. show wherein a plating layer of Ni is provided between the coating layer and the surface of the base member on which the coating layer is formed.

28. The member for a semiconductor device according to claim 14, Yamazaki et al. show wherein a plating layer of Ni is provided between the coating layer and the surface of the base member on which the coating layer is formed.

29. The member for a semiconductor device according to claim 16, Yamazaki et al. show wherein a plating layer of Ni is provided between the coating layer and the surface of the base member on which the coating layer is formed.

30. Yamazaki et al. show show a semiconductor device employing the member for a semiconductor device according to claim 12.

31. Yamazaki et al. show a semiconductor device employing the member for a semiconductor device according to claim 14.

32. Yamazaki et al. show a semiconductor device employing the member for a semiconductor device according to claim 16.

Therefore, it would be obvious to one of ordinary skill in the art to use the thickness of Hirose et al.'s coating layer to modify the thickness of Yamazaki et al.'s hard carbon coating layer for the purpose of providing a sufficient resin bonding strength to be maintained.

Response

Applicant's arguments filed 10/29/07 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claims 12, 14 and 16, " cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. ∋ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. ∋ 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. ∋ 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY

PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Field of Search	Date
U.S. Class and subclass: 257/704,707,710,778,734,737,738,641,e23,111,e23,181,e23.191,e23.116,e23.056,e23.037 174/52.4,529	4/2/07 7/29/07 1/13/08
Other Documentation: foreign patents and literature in 257/704,707,710,778,734,737,738,641,e23,111,e23,181,e23.191,e23.116,e23.056,e23.037 174/52.4,529	4/2/07 7/27/07 1/13/08
Electronic data base(s): U.S. Patents EAST	4/2/07 7/29/07 1/13/08

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
1/13/08